AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multiple memory controller system, comprising:

at least two memory controllers for controlling a main memory, wherein a first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory, wherein each of the at least two memory controllers is configured to communicate with a central processing unit via the central processing unit bus, wherein each of the memory controllers are independent of the processor, and also wherein the first of the at least two memory controllers comprises an accelerated graphics port for establishing a dedicated point-to-point connection between the first of the at least two memory controllers and an accelerated graphics processor ~~and wherein the first of the at least two memory controllers is configured to reroute requests for the other addresses to a second of the at least two memory controllers~~.

2. (Original) The system of Claim 1, wherein the first of the at least two memory controllers defines a range of addresses in memory that are preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

3. (Original) The system of Claim 1, wherein at least two of the at least two memory controllers are manufactured on the same chip.

4. (Original) The system of Claim 1, wherein the first of the at least two memory controllers maintains a graphical address remapping table comprising at least one page table entry (PTE) providing information for translation of a virtual address to a physical address, wherein the virtual address includes a first portion and a second portion, the first portion corresponding to a PTE in the graphical address remapping table and wherein the second portion and information provided by the PTE are combined to provide the physical address.

5. (Original) The system of Claim 4, wherein the first portion comprises a virtual page number field.

6. (Original) The system of Claim 4, wherein the second portion comprises an offset field.

7. (Original) The system of Claim 4, wherein the graphical address remapping table is configured by loading at least one configuration register during boot up of a computer system.

8. (Original) The system of Claim 7, additionally comprising one configuration register includes a starting address of the graphical address remapping table.

9. (Original) The system of Claim 7, wherein the at least one configuration register includes a boundary address defining the lowest address of a graphical address remapping table range.

10. (Original) The system of Claim 7, wherein the at least one configuration register includes a range register defining the amount of memory that is preferentially used over other addresses for storage of graphics data for accelerated graphic port transactions.

11. (Original) The system of Claim 7, wherein an initialization BIOS loads the at least one configuration register.

12. (Original) The system of Claim 7, wherein an operating system API loads the at least one configuration register.

13. (Original) The system of Claim 1, wherein the one of the at least two memory controllers and a memory are on a single semiconductor chip.

14. (Currently Amended) A computer, comprising:

at least one accelerated graphics processor; and

at least two memory controllers for controlling a main memory, wherein a first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory, wherein each of the at least two memory controllers is configured to communicate with a central processing unit via the central processing unit bus, wherein each of the memory controllers are independent of the processor, and ~~also~~ wherein the first of the at least two memory controllers comprises an accelerated graphics port for establishing a dedicated point-to-point connection between the first of the at least two memory controllers and the accelerated graphics processor~~, and wherein the first of the at least two memory controllers is configured to reroute requests for the other addresses to a second of the at least two memory controllers~~.

15. (Original) The system of Claim 14, wherein the first of the at least two memory controllers defines a range of addresses that are preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

16. (Original) The computer of Claim 14, wherein at least two of the at least two memory controllers include an accelerated graphics port.

17. (Original) The computer of Claim 14, wherein at least two of the at least two memory controllers are included on the same chip.

18. (Original) The computer of Claim 14, further comprising a graphical address remapping table residing on a memory connected to said first of the at least two memory controllers.

19. (Original) The computer of Claim 18, wherein the graphical address remapping table is configured by loading at least one configuration register during boot up of a computer system.

20. (Original) The computer of Claim 18, additionally comprising at least one configuration register that includes a starting address of the graphical address remapping table.

21. (Original) The computer of Claim 18, wherein the at least one configuration register includes a boundary address defining the lowest address of a graphical address remapping table range.

22. (Original) The computer of Claim 18, wherein an initialization BIOS loads the at least one configuration register.

23. (Original) The computer of Claim 18, wherein an operating system API loads the at least one configuration register.

24. (Original) The computer of Claim 14, further comprising a graphical address remapping table residing on said first of the at least two memory controllers, wherein the graphical address remapping table comprises at least one page table entry (PTE) providing information for translation of a virtual address to a physical address, wherein the virtual address includes a first portion and a second portion, the first portion corresponding to a PTE in the graphical address remapping table and wherein the second portion and the information provided by the PTE are combined to provide the physical address.

25. (Original) The computer of Claim 14, wherein the first portion comprises a virtual page number field.

26. (Original) The computer of Claim 14, wherein the second portion comprises an offset field.

27. (Original) The computer of Claim 14, wherein said first of the at least two memory controllers and a memory are on a single semiconductor chip.

28. (Currently Amended) A multiple memory controller computer comprising:

means for transmitting data to at least two memory controllers that each control a main memory wherein a first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory, and wherein each of the at least two memory controllers is configured to communicate with a central processing unit via the central processing unit bus, wherein each of the memory controllers are independent of the processor ~~wherein the first of the at least two memory controllers is configured to reroute requests for the other addresses to a second of the at least two memory controllers~~; and

means for providing a dedicated point-to-point connection between a graphics accelerator and a first of the at least two memory controllers.

29. (Original) The computer of Claim 28, and wherein the first of the at least two memory controllers defines a range of addresses that is preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

30. (Original) The computer of Claim 28, further comprising means for controlling a graphical address remapping table having at least one page table entry (PTE) providing information for a translation of a virtual address to a physical address, wherein the virtual address includes a first portion and a second portion, the first portion corresponding to a PTE in the graphical address remapping table and wherein the second portion and information provided by the PTE are combined to provide the physical address.

31. (Original) The computer of Claim 30, wherein the first portion comprises a virtual page number field.

32. (Original) The computer of Claim 30, wherein the second portion comprises an offset field.

33. (Original) The computer of Claim 30, wherein the physical address references a location in a memory.

34. (Original) The computer of Claim 33, wherein an initialization BIOS loads said at least one configuration register.

35. (Original) The computer of Claim 33, wherein an operating system API loads said at least one configuration register.

36. (Original) The computer of Claim 30, wherein the graphical address remapping table is configured by loading said at least one configuration register during boot up of a computer system.

37. (Original) The computer of Claim 28, additionally comprising at least one configuration register that includes a starting address of the graphical address remapping table.

38. (Original) The computer of Claim 35, wherein the at least one configuration register includes a boundary address defining the lowest address of a graphical address relocation table range.

39. (Original) The computer of Claim 35, wherein said at least one configuration register includes a range register defining the amount of memory that is preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

40. (Currently Amended) A method of using a multiple memory controller computer, comprising:

controlling a main memory with at least two memory controllers, wherein a first memory controller is connected to an accelerated graphics processor via a dedicated point-to-point connection, and wherein the first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory, wherein each of the at least two memory controllers is configured to communicate with a central processing unit via the central processing unit bus, wherein each of the memory controllers are independent of the processor ~~and wherein the first of the at least two memory controllers is configured to reroute requests for the other addresses to a second of the at least two memory controllers~~; and

defining a group of addresses in the main memory that are preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

41. (Original) The method of Claim 40, further comprising the act of controlling a graphical address remapping table having at least one page table entry (PTE) which provides information for a translation of a virtual address to a physical address, wherein the virtual address includes a first portion and a second portion, the first portion corresponding to a PTE in the

graphical address remapping table and wherein the second portion and information provided by the PTE are combined to provide the physical address.

42. (Original) The method of Claim 41, further comprising allocating a virtual page number field to the first portion.

43. (Original) The method of Claim 41, further comprising allocating an offset field to the second portion.

44. (Original) The method of Claim 41, further comprising loading said at least one configuration register during boot up of a computer system.

45. (Original) The method of Claim 44, further comprising defining in a base address register the starting point of memory preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

46. (Original) The method of Claim 44, further comprising setting a boundary address register defining the lowest address of the graphical address remapping table.

47. (Original) The method of Claim 44, further comprising using a range register in the at least one configuration register to define the amount of memory that is preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection.

48. (Original) The method of Claim 44, further comprising using an initialization BIOS to load said at least one configuration register.

49. (Original) The method of Claim 44, further comprising using the operating system API to load said at least one configuration register.

50. (Original) The method of Claim 40, further comprising manufacturing said at least two memory controllers and a memory on a single semiconductor chip.